High Performance Gain Cell Architecture

Abstract

A memory architecture that utilizes single-ended dual-port destructive write memory cells and a local write-back buffer is described. Each cell has separate read and write ports that make it possible to read-out data from cells on one wordline in the array, and subsequently write-back to those cells while simultaneously reading-out the cell on another wordline in the array. By implementing an array of sense amplifiers such that one amplifier is coupled to each read bitline, and a latch receiving the result of the sensed data and delivering this data to the write data lines, it is possible to ' pipeline' the read-out and write-back phases of the read cycle. This allows for a write-back phase from one cycle to occur simultaneously with the read-out phase of another cycle. By extending the operation of the latch to accept data either from the sense amplifier, or from the memory data inputs, modified by the column address and masking bits, it is also possible to pipeline the read-out and the modify-write-back phases of a write cycle, allowing them to occur simultaneously. The architecture preferably employs a nondestructive read memory cell such as 2T or 3T gain cells, achieving an SRAM-like cycle and access times with a smaller and more SER immune memory cell.